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09/652,044	08/31/2000	Toshimitsu Taniguchi	10417-039001	2951

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Applicati n No. 09/652,044	Applicant(s) TANIGUCHI ET AL	
	Examiner Samuel A Gebremariam	Art Unit 2811	

– Th MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rej ctions - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 6, 7 and 29-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the specification for "forming a body layer of the first conductive type continuous with the source layer and low concentration drain layer".

Claim Objections

3. Claim 21 is objected to because of the following informalities: the limitation of "said first MOS transistor includes a micro MOS transistor; and said second MOS transistor includes a micro MOS transistor" as recited in claim 21 is not clear what it means. Is applicant trying to say the MOS transistor is a micro MOS transistor?

4. Claims 31 and 32 recite the limitation "second conductive layer" in line 2 of the claims. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim R jections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 22-26, are rejected under 35 U.S.C. 102(e) as being anticipated by Shida, US patent No. 6,033,944.

Regarding claim 22, Shida teaches (figs. 2A to 2d and fig. 3) a method of manufacturing a semiconductor device comprising: forming a source/drain regions (9) of a second conductive type in a semiconductor of a first conductive type (1); doping impurities of the first conductive type by ion implantation to form a semiconductor layer (3) of first conductive type comprising a channel located between the source/drain regions; doping impurities of the second conductive type (N^- region) into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer.

Regarding claim 23, Shida teaches (figs. 2A to 2d and fig. 3) a method of manufacturing a semiconductor device comprising: forming a low concentration source/drain regions (N^- region) of a second conductive type in a semiconductor of a first conductive type (1), forming a high concentration source/drain regions (9) of the second conductive type in the low concentration source/drain regions: doping impurities

of the first conductive type into the semiconductor of the first conductive type by ion implantation to form the semiconductor layer of the first conductive type (3) comprising a channel located between the source/drain regions; and doping impurities of the second conductive type into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer (4).

Regarding claim 24, Shida teaches (figs. 2a-2d and fig. 3) the entire claimed process of claim 23 above including the low concentration source/drain regions surround the high concentration source/drain regions and forming a gate electrode (10) on a gate oxide film (6) provided on the semiconductor of the first conductive type wherein the low concentration source/drain regions extends from under the gate electrode.

Regarding claims 25 and 26, Shida teaches (figs. 2a-2d and fig. 3) the entire claimed process of claim 24 above including the low concentration source/drain regions (N^- region) of the second conductive type are formed to be adjacent to the semiconductor layer (3) of the first conductive type formed below the gate electrode by ion implantation.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-8, 10, 11, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al. US patent No. 5,567,629.

Regarding claim 6, Kao teaches (fig. 16) a method of manufacturing a semiconductor device comprising: forming a high concentration source/drain layers (42) and (44) of a second conductive type in a semiconductor layer (12), forming a gate electrode (38) formed on a channel layer located between the source and drain layers (fig. 14), and forming a body layer (32) of the first conductive type continuous with the source layer (42) and a low concentration drain layer (19) of the second conductive type formed between the channel layer and the drain layer, wherein the body layer is formed only under the gate electrode, and wherein forming a body layer of the first conductive type comprises a step of doping impurities of the first conductive type into the semiconductor layer by ion implantation (col. 5, lines 7-18).

Regarding claims 7, 8 and 16, Kao teaches (fig. 16) substantially the entire claimed process of claim 6 above including the steps of doping impurities of the second conductive type into the semiconductor layer to form a low concentration drain layer (fig. 5) of the second conductive type; doping impurities of the second conductive type into the semiconductor layer to form a high concentration source layer (42) of the second conductive type so that the source layer is adjacent to one end of the gate electrode (38) and form a high concentration drain layer (44) of the conductive type in a position apart from the other end of the gate electrode; doping impurities of a first conductive type into the semiconductor layer to form a body layer (32) of the first conductive type extended from under one end of the gate electrode and formed so that the body layer is

continuous to the source layer (42) of the second conductive type; and forming a gate electrode (38) on a gate oxide film (14) after the gate oxide film is formed on the semiconductor layer.

Regarding claims 10 and 17, Kao teaches substantially the entire claimed process of claims 6 and 7 above including forming a gate electrode (38) on a gate oxide (14) so that the gate electrode covers the body layer (32); doping impurities of first conductive type into the layer of the second conductive type to form a body layer (32) of first conductive type by doping impurities of the conductive type as claimed using ion implantation.

Regarding claim 11, Kao teaches substantially the entire claimed process of claim 10 above including doping an impurity for forming the second conductive type layer by ion implantation after forming the body layer (Kao, figs. 15 and 16).

Regarding claim 29, Kao teaches substantially the entire claimed process of claim 10 above including the body layer (32) is continuous with the source/drain regions (42/44) regions of the second conductive type.

Claim 9, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Chen et al. US patent No. 5,926,712.

Kao teaches substantially the entire claimed process of claim 7 above except explicitly stating that the low concentration drain layer of the second conductive type or the low concentration source/drain layers of the second conductive type are formed so that they are shallow under the gate electrode and they are deep under the high

concentration drain layer of the reverse conductive type or the high concentration source/drain layers of the reverse conductive type.

It is conventional and also taught by Chen forming a low concentration drain layer (216) that is shallow under the gate and deeper under the high concentration drain region as claimed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the low concentration drain layer taught by Chen in the method of Kao.

Claims 12-15, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Shida US patent No. 6,033,944.

Regarding claims 12 and 14, Kao teaches substantially the entire claimed process of claim 10 above including forming a first gate electrode (38) for a MOS transistor on a gate oxide (14) after the gate oxide film is formed on the substrate (12) and forming source/drain layers (42/44) of the second conductivity type so that they are adjacent to the first gate electrode (38). Further Kao teaches forming more than one transistor (col. 5, lines 15-18).

Kao does not explicitly teach forming a second gate electrode for a second MOS transistor on the body layer of the first conductive type. Kao does not teach using a resist film in an area except areas where the source and drain layers of the MOS transistors are formed as a mask.

The use of resist mask is conventional in the art and Shida also teaches using a resist film (16) in an area except areas where the source and drain layers (9) of the NMOS transistors are formed as a mask (fig. 2(C), col. 7, lines 51-67)).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of resist film as a mask taught by Shida in the process of Kao in order to form both NMOS and PMOS transistors.

Regarding claims 13,15, 18 and 19, Kao teaches substantially the entire claimed process of claims 12 and 14 above including an implantation is used for forming a second conduction type (19), doping impurities of a first conductive type to form a body layer (32).

Regarding claim 20, Kao teaches substantially the entire claimed process of claims 12 and 14 above including the first MOS transistor is a micro MOS transistor; and the second MOS transistor is a micro MOS transistor having high resistance to voltage.

The limitation that the above transistor is a micro MOS is conventional device that is commonly fabricated in semiconductor fabrication.

With regards to the limitation that the MOS transistor have a high resistance to voltage, this characteristic is considered to be inherent characteristic of most transistors since any layer have a resistance to voltage value.

Regarding claim 30, Kao teaches substantially the entire claimed process of claims 12 and 14 above including the body layer (32) is continuous with the source/drain regions (42/44) regions of the second conductive type.

Regarding claims 31 and 32, Shida teaches substantially the entire claimed process of claims 22 and 23 above including the second conductive type layer (N^- region) is continuous with source/drain regions of the second conductive type layer.

Regarding claim 33, Shida teaches substantially the entire claimed process of claim 24 above including the channel is continuous with the source/drain regions (9) of the second conductive type.

Claims 27 and 28, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo in view of Shida.

Regarding claims 27 and 28, Kubo teaches substantially the entire claimed process of claims 12 and 22-26 above including doping impurities using a resist film, as a mask, to form first and second MOS transistors.

Kubo teaches forming an n-channel MOSFET. It is within one of ordinary skill in the art to realize that it only takes reversing the polarity of the dopants to form p-channel MOSFET.

Furthermore it is conventional and also taught by Shida to form more than one transistor as claimed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form more than one MOS transistor in order to make a functional device.

The limitation the semiconductor device comprising a first transistor having high resistance to voltage and a second transistor having high resistance to voltage is not taught Kubo explicitly.

The claimed characteristic is considered to be inherent characteristic of most transistors since any layer have a resistance to voltage value.

Response to Arguments

7. Applicant's arguments with respect to claims 6-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 305-7646. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
July 25, 2003

Steven Loke
Primary Examiner